IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Moeckly et al.	Examiner:	Paul A. Wartalowicz
Serial No.:	10/751,091	Group Art Unit:	1754
Filed:	01/02/2004	Docket No.:	10467.0043USI2
Title:	HIGH-TEMPERATURE SUPERCONDUCTOR DEVICES AND METHODS OF FORMING THE SAME		

CERTIFICATE UNDER 37 CFR 1.8:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 July 5, 2007.

By:
Name: Lisa Hill

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT (37 C.F.R. § 1.97(b))

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

With regard to the above-identified application, the items of information listed on the enclosed Form 1449 are brought to the attention of the Examiner.

This statement should be considered because it is submitted before the mailing date of a first Office Action on-the-merits. Accordingly, no fee is due for consideration of the items listed on the enclosed Form 1449.

In accordance with 37 C.F.R. §1.98(d), a copy of each document or other information listed on the enclosed Form 1449 is not provided because it was previously cited by or submitted to the U.S. Patent and Trademark Office in parent application, U.S. Serial No. 10/704,215 filed on November 6, 2003.

No representation is made that a reference is "prior art" within the meaning of 35 U.S.C. §§ 102 and 103 and Applicants reserve the right, pursuant to 37 C.F.R. § 1.131 or otherwise, to establish that the reference(s) are not "prior art." Moreover, Applicants do not represent that a reference has been thoroughly reviewed or that any relevance of any portion of a reference is intended.

Consideration of the items listed is respectfully requested. Pursuant to the provisions of M.P.E.P. 609, it is requested that the Examiner return a copy of the attached Form 1449, marked as being considered and initialed by the Examiner, to the undersigned with the next official communication.

Please charge any additional fees or credit any overpayment to Deposit Account No. 13-2725.

Respectfully submitted,

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Date: July 5, 2007

By _____
Tong Wu
Reg. No. 43,361

Date Mailed: July 5, 2007

FORM 1449 INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION (Use several sheets if necessary)	Docket Number: 10467.43USI2	Application Number: 10/751,091
	Applicant: MOECKLY ET AL.	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4,916,116	04/10/1990	Yamazaki			
	4,943,558	07/24/1990	Soltis et al.			
	5,077,270	12/31/1991	Takeda et al.			
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	5,696,392	12/09/1997	Char et al.			
	5,892,243	04/1999	Chan			
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FOREIGN PATENT DOCUMENTS

	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		"Poster Sessions", *Source Unknown*, pg. 109 (1994)
		Agostinelli, J. et al., "Cubic Phase in the Y-Ba-Cu-O System", *Physical Review B*, Vol. 43, No. 13, pp. 11 396-11 399 (May 1991)
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		Hunt, B. et al., "High Temperature Superconductor Josephson Weak Links", *Second Symposium on Low Temperature Electronics and High Temperature Superconductivity, Electrochemical Society Meeting, Honolulu, Hawaii*, Vol. 93-22, pp. 467-472 (May 1993).
		Hunt, B.D. et al., "High-T_c Superconductor/normal-metal/superconductor Edge Junctions and SQUIDs with Integrated Groundplanes", *Appl. Phys. Lett.*, Vol. 68, No. 26, pp. 3805-3807 (June 24, 1996).
		Ishimaru, Y. et al., "Evaluation of fabrication process and barrier structure for interface-modified ramp-edge junctions," *Physica C*, Vol. 378-381, pp. 1327-1333 (2002).
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		Mallison, W. H. et al., "A multilayer $YBa_2Cu_3O_x$ Josephson Junction Process for Digital Circuit Applications", *Appl. Phys. Lett.*, Vol.. 68, No. 26, pp. 3808-3810 (June 24, 1996).
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		Moeckly B. H. et al., "Properties of Interface-engineered High T_c Josephson Junctions", *Appl. Phys. Lett.*, Vol. 71, No. 17 , pp. 2526-2528 (October 27, 1997)
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		Yoshida, J., "Recent Progress of High-Temperature Superconductor Josephson Junction Technology for Digital Circuit Applications," *IEICE Trans. Electron.*, Vol. E83-C, No. 1, pp. 49-59 (January 2000).
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